A1 Concl'd

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied form the address-input circuit.

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A2

39 ~~21~~. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and [The memory circuit as claimed in claim 18, wherein]

the strobe signal has a cycle identical to that of the clock signal, and a first timing of a first rising edge of the strobe signal is different from a second timing of a corresponding rising edge of the clock signal.

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A3

41. (Amended) A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal, said address-input circuit includes a shift register which operates in response to the clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

A3

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit;

said timing signal is responsive to the clock signal; and

[The memory circuit as claimed in claim 32, further comprising] a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.

42. (Amended) A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal, the address-input circuit includes a shift register which operates in response to the clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit;

the said timing signal is responsive to the strobe signal; and

[The memory circuit as claimed in claim 33, further comprising]

a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.

## REMARKS

The above amendments and the following remarks are responsive to the Office Action dated February 3, 2000. Claims 1-42 are pending in this application. In the outstanding Office Action, claims 18-20, and 23-40 were rejected under 35 U.S.C. § 102(b); claims 1-17 were allowed; and claims 21, 22, 41 and 42 were objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 18, 21, 41, and 42 were amended without adding any new matter. With the allowance of claims 1-17, claims 18-42 are submitted for consideration.

**35 U.S.C. § 102(b)**

Claims 18-20 and 23-40 were rejected under 35 U.S.C. § 102(b) as being anticipated by Fukuzo. In Fukuzo, the latch circuits 32d and 32i, which the Office Action equates to the address-input circuit of claim 18, latches signals Drow and Dcol in response to the timing control signals CTL1 and CTL2, respectively. Similarly, the Office Action equates the latch circuit 33e of Fig. 2 of Fukuzo to the data-input circuit of claim 18. Latch circuit 33e latches signal Din upon receipt of latch control signal CTL3.

Claim 18 covers a memory circuit receiving a clock signal and a strobe signal which have an identical cycle but have independent timings. This circuit requires: an address-input circuit which latches address signals in response to the clock signal, and outputs the address signals in response to a timing signal; a data-input circuit which latches data signals in response to the strobe signal, and outputs the data signals in response to said timing signal; and an internal circuit which writes the data signals supplied from the data-



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input circuit in memory cells indicated by the address signals supplied form the address-input circuit.

It is apparent from the claim language that this timing signal is different from the clock signal that is used for latching the address signals. Nowhere in the specification or drawings does Fukuzo teach that latch circuits 32d and 32i output address signals in response to a timing signal that is different from the timing control signals CTL1 and CLT2. Namely, there is no mention, whatsoever, of a timing signal that is different from the timing control signals CTL1 and CLT2.

Accordingly, Fukuzo neither teaches or suggests an address-input circuit which latches address signals in response to the clock signal, and outputs the address signals in response to a timing signal.

Similarly, the Office Action equates the latch circuit 33e of Fig. 2 of Fukuzo to the data-input circuit of claim 18. Nowhere in the specification or drawings does Fukuzo teach that latch 33e outputs the data signal in response to a timing signal that is different from the timing control signal CTL3. Namely, there is no mention, whatsoever, of a timing signal that is different from the timing control signal CTL3.

Consequently, Fukuzo neither teaches nor suggests a data-input circuit which latches data signals in response to the strobe signal, and outputs the data signals in response to the timing signal.

Further, as clearly set forth in claim 18 as amended, the timing signal is used by both the address-input circuit and the data-input circuit for outputting the address signals and the data signals, respectively. In Fukuzo, on the other hand, Fig. 2 clearly shows that each of the latch circuits 32d, 32i or 33e receive a different latch control signal.



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